Technology of MISFET with SiO\textsubscript{2}/BaTiO\textsubscript{3} System as a Gate Insulator

Piotr Firek and Jan Szmidt

Abstract—The properties of barium titanate (BaTiO\textsubscript{3}, BT), such as high dielectric constant and resistivity, allow it to find numerous applications in the field of microelectronics. In this work silicon metal-insulator-semiconductor field effect transistor (MISFET) structures with BaTiO\textsubscript{3} thin films (containing La\textsubscript{2}O\textsubscript{3} admixture) acting as gate insulator were investigated. The films were produced by means of radio frequency plasma sputtering (RF PS) of sintered BaTiO\textsubscript{3} + La\textsubscript{2}O\textsubscript{3} (2\% wt.) target. In the paper transfer and output $I-V$, transconductance and output conductance characteristics of the obtained transistors are presented and discussed. Basic parameters of these devices, such as threshold voltage ($V_{TH}$) are determined and discussed.

Keywords—barium titanate, $I-V$ characteristics, MISFET structures, radio frequency plasma sputtering.

1. Introduction

Barium titanate (BaTiO\textsubscript{3}, BT) ceramics have been extensively used in the field of electronic applications. Multilayer ceramic capacitors (MLCCs) [1], [2], embedded capacitances in printed circuit boards [2], optical waveguides [3], electrooptic modulators [4], micromechanical [5] and humidity sensor [6] devices, positive temperature coefficient of resistivity thermistors [7], gas sensors [8] were fabricated using BT. In all those applications BaTiO\textsubscript{3} was used in the form of either bulk material or thick layer. BT shows ferroelectric and piezoelectric properties as well as a high dielectric constant that make it a promising material for potential applications in dynamic access random memories (DRAM) [9], [10] or non-volatile memories (NVM) [9], [11].

Thin barium titanate films for microelectronic applications are usually either amorphous or polycrystalline and have significantly worse electrical properties than bulk or thick-film material. It is difficult, for example, to obtain uniform composition, the piezoelectric effect is weaker, and the values of the dielectric constant are lower (typically less then 50) [12]. On the other hand, its dielectric constant is usually still much higher than that of silicon dioxide although thin BT layers are typically plagued with higher leakage current and lower dielectric strength.

2. Experimental Details

The fabrication process of metal-insulator-semiconductor field effect transistor (MISFET) structures is presented...
in Fig. 1. Its first step is thermal oxidation in order to obtain field oxide of about 440 nm. The p-type silicon $<100>$ oriented substrate with the resistivity of $6 - 8 \Omega \cdot cm$ was used. After cleaning processes 40 nm thick SiO$_2$ film was grown thermally and then a thin (approximately 80 nm) barium titanate film was deposited by means of radio frequency plasma sputtering (RF PS) of sintered BaTiO$_3$ + La$_2$O$_3$ (2% wt.) target.

A schematic diagram of the RF PS setup is shown in Fig. 2. The BaTiO$_3$ layer was deposited as a result of 30 min long process (280 V self-bias voltage, argon flow rate of 10 ml/min and 15 mm distance between the Si substrate and the sputtered target). Next, a photoresist mask for etching in a buffer solution of hydrofluoric acid was prepared by means of photolithography. As a last step contacts for metallization were opened and aluminum was evaporated. The described fabrication process is presented in Fig. 2. Silicon wafer and transistor topography are shown in Fig. 3.

3. Results and Discussions

The dielectric constant ($k$) of about 20 was extracted from capacitance-voltage measurements of a MIS structure containing BaTiO$_3$ dielectric. The current-voltage ($I - V$) characteristics of MISFETs were measured with Keithley SMU 236/237/238. The obtained transfer and output characteristics are presented in Figs. 4 and 5.

![Fig. 2. Schematic diagram of the setup for radio frequency plasma sputtering deposition processes.](image)

![Fig. 3. Silicon wafer and MISFET topography.](image)

![Fig. 4. Transfer current-voltage characteristics of the fabricated structures.](image)

![Fig. 5. Output current-voltage characteristics of the fabricated structures.](image)
Threshold voltage ($U_T$) is one of the most important parameters of a transistor since it represents the gate voltage at which the MISFET channel is turned on. The threshold voltage ranged from $-6$ V to $-8$ V.

The transconductance $g_m$ and output conductance of the structures are presented in Figs. 6 and 7, respectively.

**4. Conclusions**

The obtained BT films show good adhesion to SiO$_2$ layers on silicon substrate. Their relatively low dielectric constant ($k$) for BT is due to its amorphous nature. High values of the threshold voltage are a consequence of charge presence at the SiO$_2$/BaTiO$_3$ interface. A better control of the deposition process (e.g., purity) may significantly improve the film properties. Our investigations confirm that the RF PS method is suitable for obtaining BT layers that may exhibit several very interesting electronic properties, especially for future IS (ion sensitive) FET structures.

**References**


Piotr Firek and Jan Szmidt


Piotr Firek was born in Rawa Mazowiecka, Poland, in 1977. He received the M.Sc. degree in microelectronics from the Faculty of Electronics and Information Technology, Warsaw University of Technology (WUT), Poland, in 2004, where he is currently finishing a Ph.D. thesis. His research concentrates on fabrication, characterization, processing and application of thin and thick film materials (e.g., barium titanate, boron nitride, DLC, diamond) in microelectronic devices.

e-mail: pfirek@elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland

Jan Szmidt received the M.Sc. degree in electronics from the Faculty of Electronics, Warsaw University of Technology (WUT), Poland, in 1976. From the same university, he received the Ph.D. and D.Sc. degrees in 1984 and 1995, respectively. In 1999, he became an Associate Professor. In 2002 he became an Associate Dean for Development of the Faculty of Electronics and Information Technology, Warsaw University of Technology. Since 2006 he has been the Head of Electronic Materials and Microsystem Technology Division, Institute of Microelectronics and Optoelectronics, WUT and since 2008 – the Dean of the Faculty of Electronics and Information Technology WUT. His research interests concentrate on technology and characterization of thin films for electronics, especially for microelectronics and nanoelectronics, as well as on their application in microelectronic and nanoelectronic structures.

e-mail: j.szmidt@elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland